IDEC Chip Design Contest

32-bit Processor with Posit Arithmetic Coprocessor for Embedded Systems

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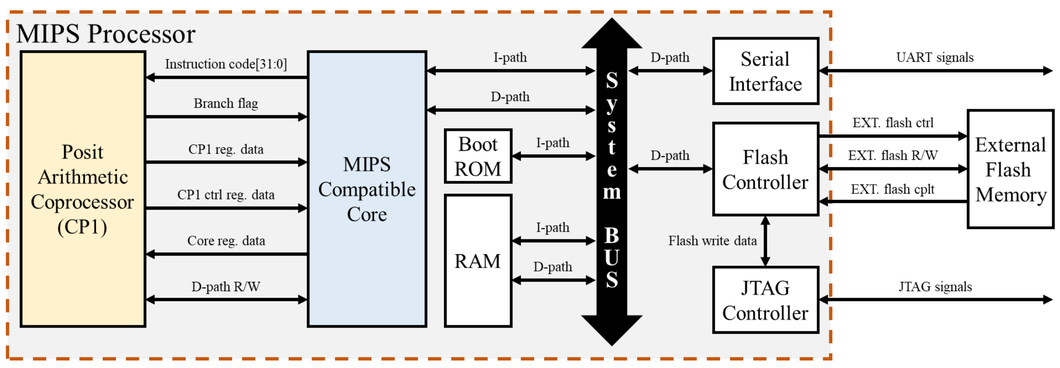
Abstract

We propose a 32-bit processor with a floating-point coprocessor. The proposed processor adopts MIPS instruction set architecture (ISA) and the coprocessor is based on posit number system. We fabricate the processor with Samsung 28nm CMOS technology.

Architecture

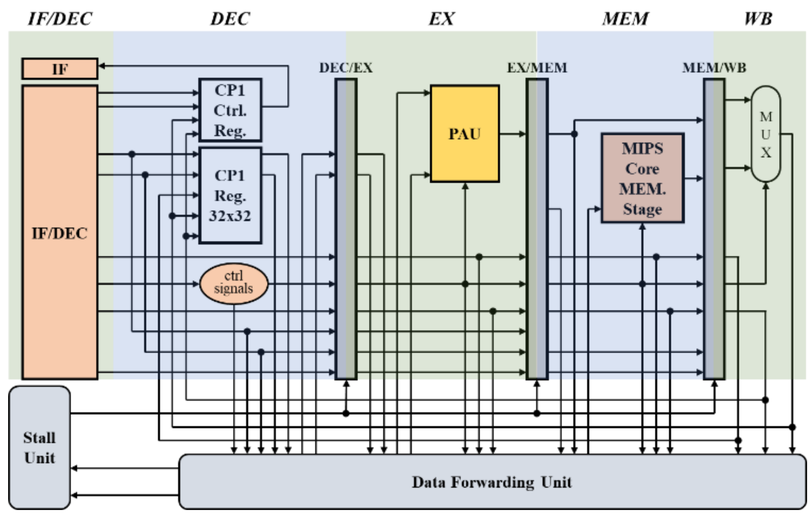
The system with our processor consists of 32-bit MIPS processor and external flash memory.



[Architecture of the proposed processor]

1) MIPS Compatible Core

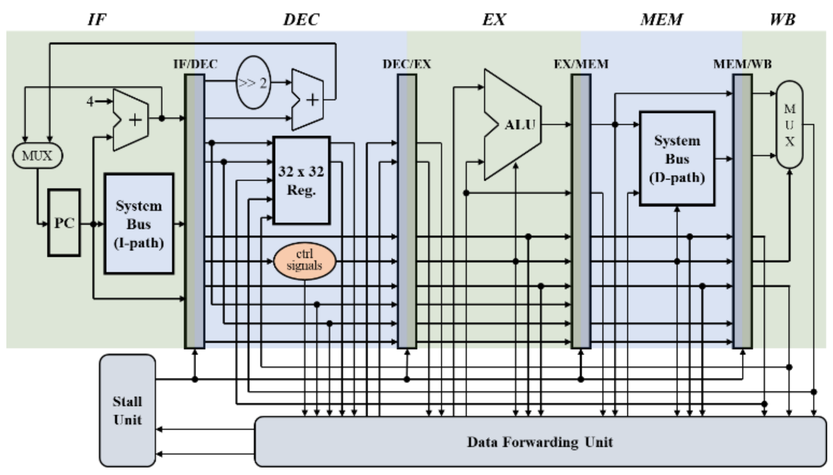
The core includes thirty-two 32-bit general-purpose registers (GPR), 5-stage pipelines, data forwarding unit, and stall unit.



[MIPS compatible core]

2) Posit Arithmetic Coprocessor

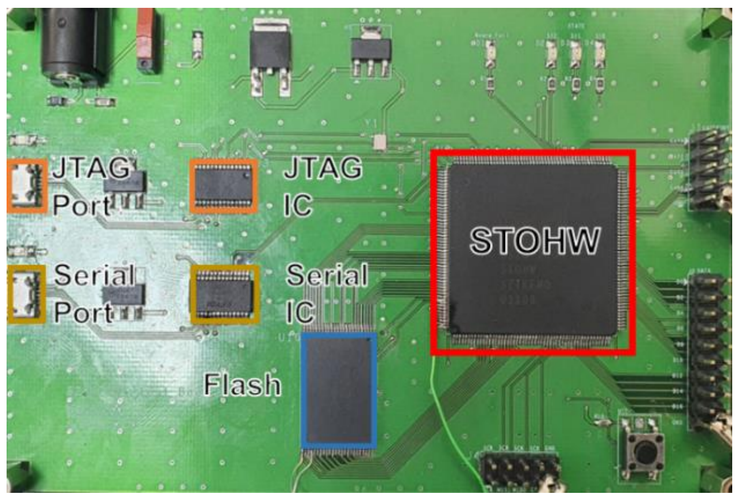
The coprocessor provides 32-bit, es=3 posit arithmetic features with 32 of 32-bit coprocessor registers which are called CP1R. The difference between the core and the coprocessor is that the ALU, in coprocessor, is replaced with 32-bit posit arithmetic unit (PAU).



[Posit arithmetic coprocessor]

Chip Verification

- In order to verify the chip with proposed design, we designed the PCB and mount the chip to the designed PCB.
- The JTAG and flash controller on proposed processor work as intended, however, register-transfer level (RTL) error exists on the flash controller and should be fixed.
- Thus, we verified the posit coprocessor and the MIPS processor utilizing pre-programmed flash memory and checking the printed results.



[Verification prototype]

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Functionality Test
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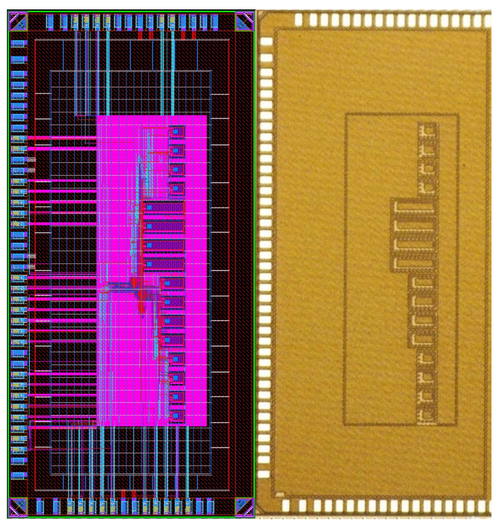
i1 = 0x50
i2 = 0x23
f1 = i1 / i2 = 0x44924924 = 2.28571402
f2 = i2 / i1 = 0x3B000000 = 0.43750000
 f1 + f2 = 0x45724924 = 2.72321406
 f1 - f2 = 0x43649248 = 1.84821402
 f1 * f2 = 0x3FFFFFFF = 0.99999994
 f1 / f2 = 0x49397829 = 5.22448926
-f1 + f2 = 0xC3649248 = -1.84821402
-f1 - f2 = 0xC5724924 = -2.72321406
-f1 * f2 = 0xBFFFFFFF = -0.99999994
-f1 / f2 = 0xC9397829 = -5.22448926
sqrt(f1) = 0x420D4C77 = 1.51298698
int32_t(f1) = 2
int32_t(f2) = 0
int32_t(f1 + f2) = 2
posit32(1) = 0x40000000 = 1.00000000
f1 != f2
f1 > f2
f1 >= f2
```

[Verification results]

Chip Implementation



[Chip layout and photograph]

Chip specification

Technology	28nm CMOS
Core Voltage	1.0V
I/O Voltage	1.8V
Chip Size	4mm x 2mm
Operating Frequency	50MHz
Area	2140,830μm^2
Power Consumption	3.74mW
Operating Temperature	-40℃~125℃

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.